



Patent Application  
Attorney Docket No.: 57941.000062  
Client Reference No.: RA001.2003.1.C.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :  
:   
Michael FARMWALD et al. :   
: Group Art Unit: Unassigned  
Appln. No.: 10/716,595 :   
: Examiner: Unassigned  
Filed: November 20, 2003 :   
:   
For: INTEGRATED CIRCUIT I/O USING :   
A HIGH PERFORMANCE BUS :   
INTERFACE :

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicant(s) hereby submits attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-

identified patent application. Applicant(s) hereby expressly reserves the right to swear behind the effective dates of any of the cited references. Applicant(s) further reserves the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the best references of which the associated individuals are aware.

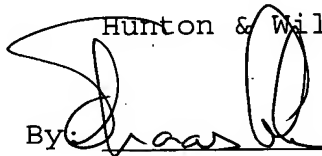
The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicant(s).

Since copies of the cited references were previously submitted in prior U.S. Patent Application No. 09/801,151, copies of the cited references are not being submitted herewith. However, copies will be forwarded at the request of the Examiner.

In accordance with 37 CFR § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified patent application entered the national stage as set forth in 37 CFR § 1.491; or (iii) before the mailing date of a first Office Action on the merit for the above-identified patent application. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

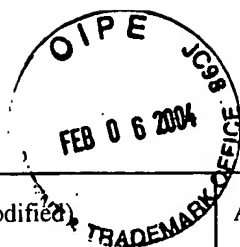
Respectfully submitted,

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Date: February 6, 2004



PTO-1449 (Modified)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 57941.000062	SERIAL NUMBER 10/716,595
	APPLICANT(S) MICHAEL FARMWALD ET AL.	
	FILING DATE November 20, 2003	GROUP ART UNIT Unassigned

## U.S. PATENT DOCUMENTS

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	2.	4,703,418	Oct. 27, 1987	James			
	3.	4,726,021	Feb. 16, 1988	Horiguchi et al.			
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	6.	S56-82961	July 7, 1981	Japan			YES
	7.	S57-14922	Jan. 26, 1982	Japan			YES
	8.	Sho 60-80193	May 8, 1983	Japan			YES
	9.	Sho 60-55459	Mar. 30, 1985	Japan			YES
	10.	S61-72350	April 14, 1986	Japan			YES
	11.	S63-142445	June 14, 1988	Japan			YES
	12.	B63-46864	Sept. 19, 1988	Japan			YES
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EXAMINER	DATE CONSIDERED
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	25.	European Search Report for EPO Patent Application No. 00 101 1832
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	27.	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
	28.	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
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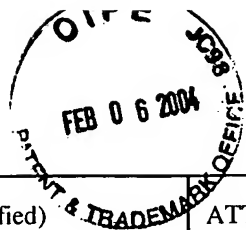
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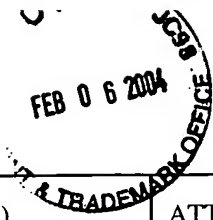
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	98.	EP 0424774	05/02/91	EPO			
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	111.	JP-A-1- 236494	09/21/89	JP			YES
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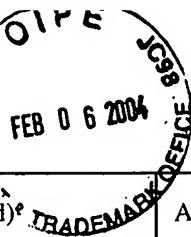
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	APPLICANT(S) MICHAEL FARMWALD ET AL.	
	FILING DATE November 20, 2003	GROUP ART UNIT Unassigned

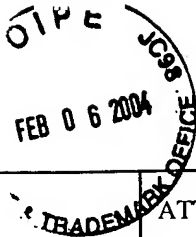
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	163.	SHO 58-192154	Nov. 9, 1983	Japan			NO
	164.	SHO 63-34795	Feb. 15, 1988	Japan			NO
	165.	SHO 61-107453	May 26, 1986	Japan			NO
	166.	SHO 63-91766	April 22, 1988	Japan			YES
	167.	SHO 62-16289	Jan. 24, 1987	Japan			NO
	168.	SHO 61-160556	Oct. 4, 1986	Japan			NO
	169.	JP 1284132	Nov 15, 1989	Japan			YES

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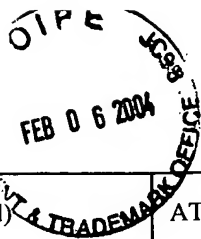
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